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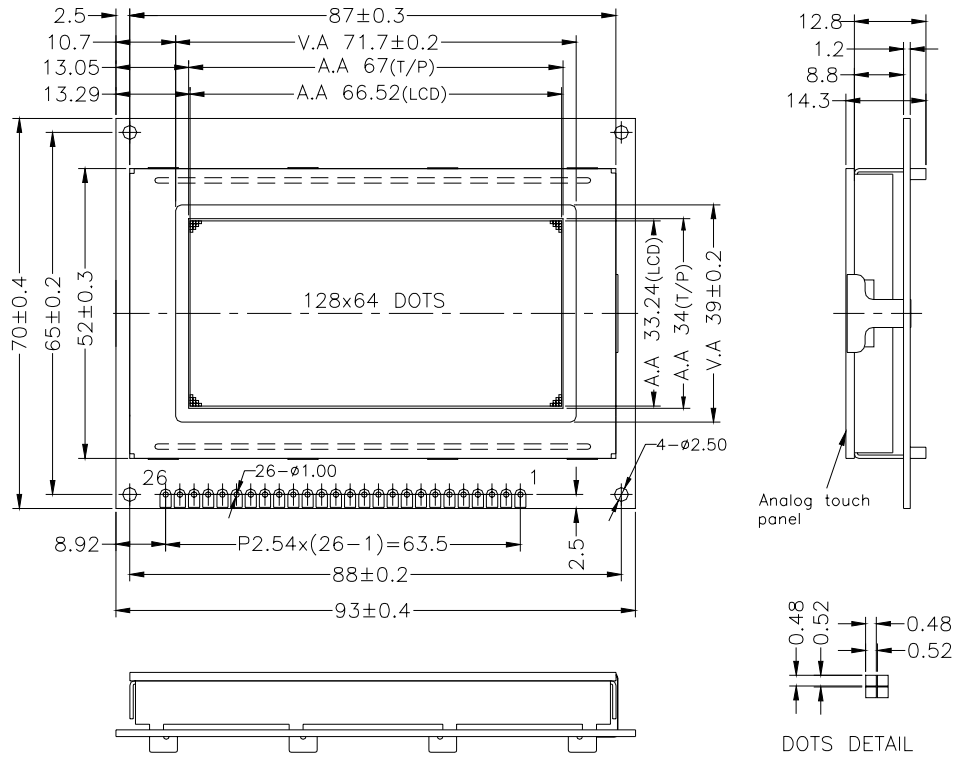
LCD

HDEM 128 64 LCD
grafikus 128x64
FSTN

2020.01.22

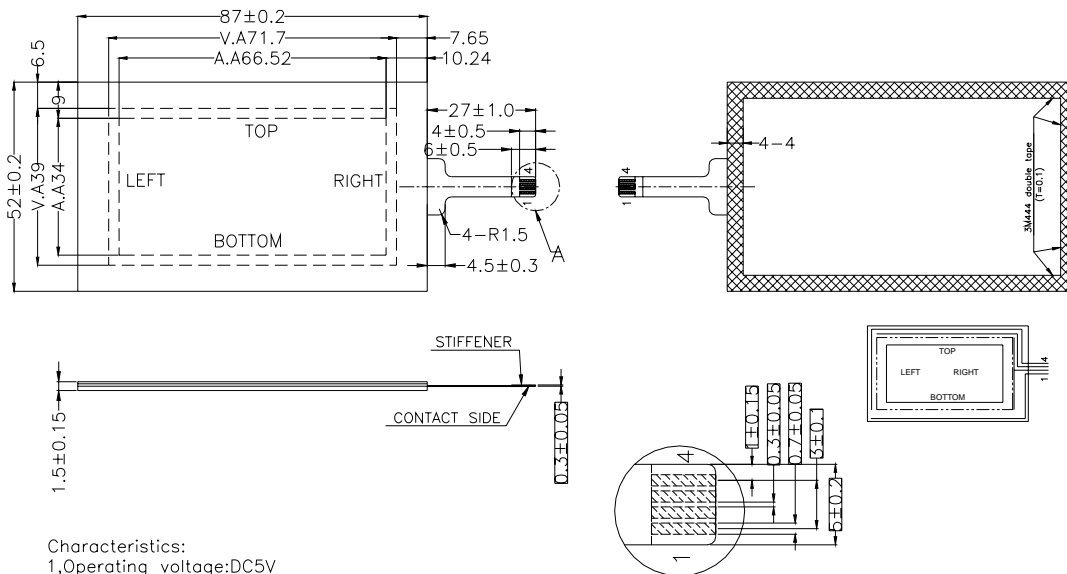
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3. EXTERNAL DIMENSIONS



REMARKS:
 1, UNMARKED TOLERANCE IS ± 0.3
 2, THE MATERIAL COMPLY WITH RoHS

4. TOUCH PANEL DRAWING



Characteristics:
 1, Operating voltage: DC5V
 2, Operating pressure: 30~70g
 3, Linearity: $\pm 1.5\%$ or less
 4, Operating temperature: $-20^{\circ}\text{C} \sim +70^{\circ}\text{C}$
 5, Storage temperature: $-25^{\circ}\text{C} \sim +75^{\circ}\text{C}$
 6, Humidity: $< 90\% \text{RH}$
 7, Transmittance: 75% or more
 8, Connector: FPC
 9, Film Type: Anti_Glare
 10, Lifetime: 1000000 times
 11, Response time: $< 10 \text{ms}$

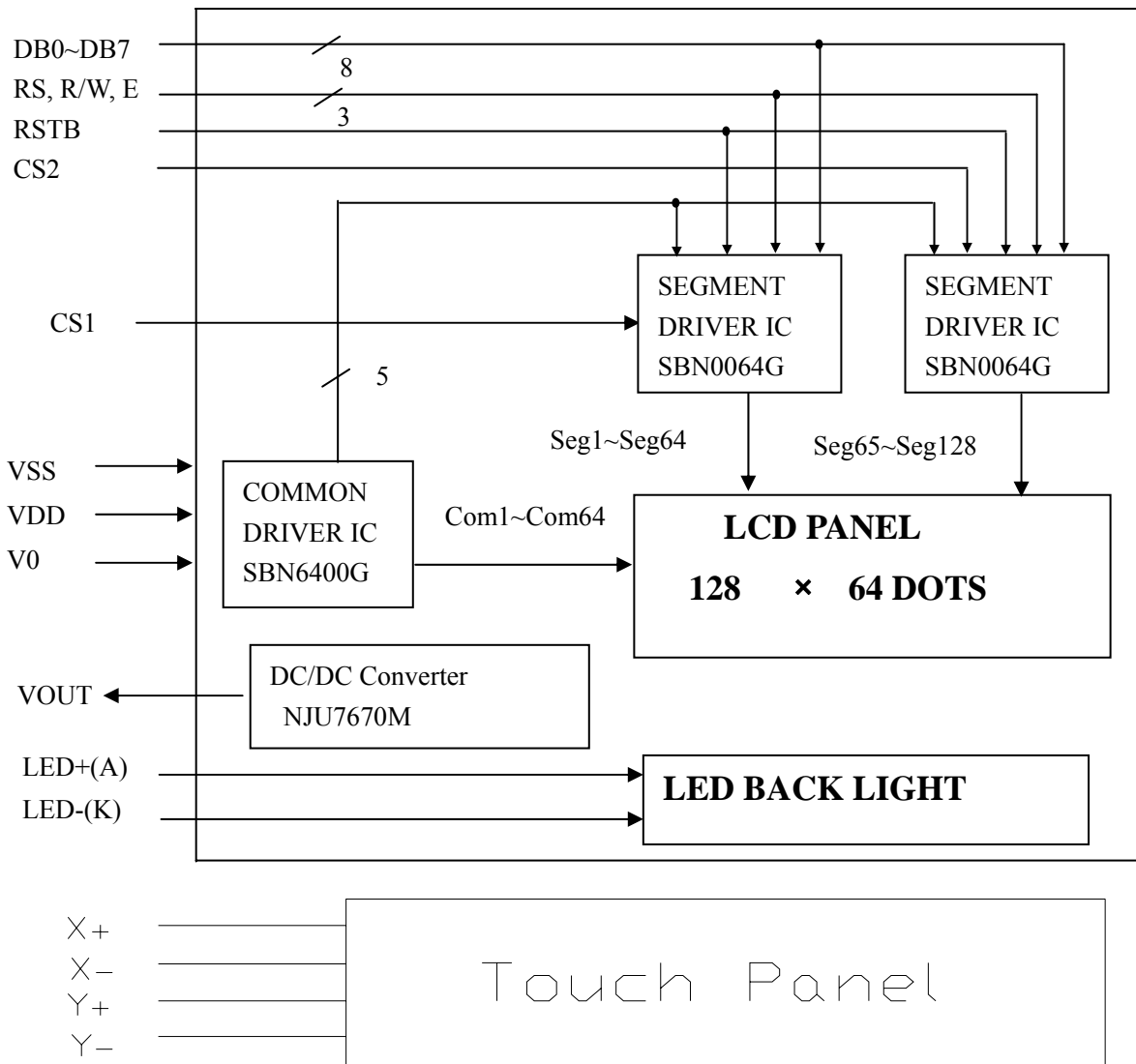
TOUCH PANEL	
No	SYMBOL
1	BOTTOM
2	RIGHT
3	TOP
4	LEFT

Detail A

Remarks:
 1, Unmarked tolerance is ± 0.3 ,
 2, The material comply with RoHS.

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5. BLOCK DIAGRAM



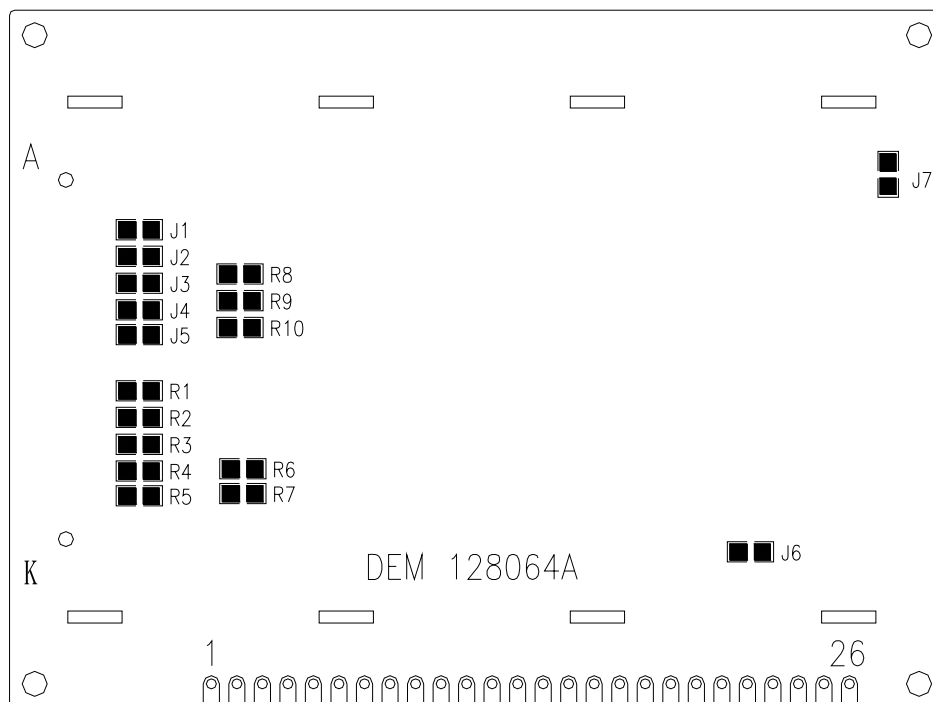
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6. PIN ASSIGNMENT

Pin No.	Symbol	Function
1	Y-	Y- Position input.
2	X-	X- Position input.
3	Y+	Y+ Position input
4	X+	X+ Position input.
5	VSS	Ground
6	VDD	Power supply voltage for logic,+ 5.0V.
7	V0	Input voltage for LCD
8	RS	Register select RS = 0...Instruction register RS = 1...Data register
9	R/W	Read /Write R/W = 1...Read R/W = 0...Write
10	E	Chip enable signal
11	DB0	Data bit 0
12	DB1	Data bit 1
13	DB2	Data bit 2
14	DB3	Data bit 3
15	DB4	Data bit 4
16	DB5	Data bit 5
17	DB6	Data bit 6
18	DB7	Data bit 7
19	CS1	Chip select signal for SBN0064G(1)
20	CS2	Chip select signal for SBN0064G(2)
21	RSTB	Reset signal
22	VOOUT	Output voltage for LCD,-9.5V
23	LED+(A)	Please also refer to 6. PCB drawing and description.
24	LED-(K)	
25	NC	No connection
26	NC	No connection

7. PCB DRAWING AND DESCRIPTION

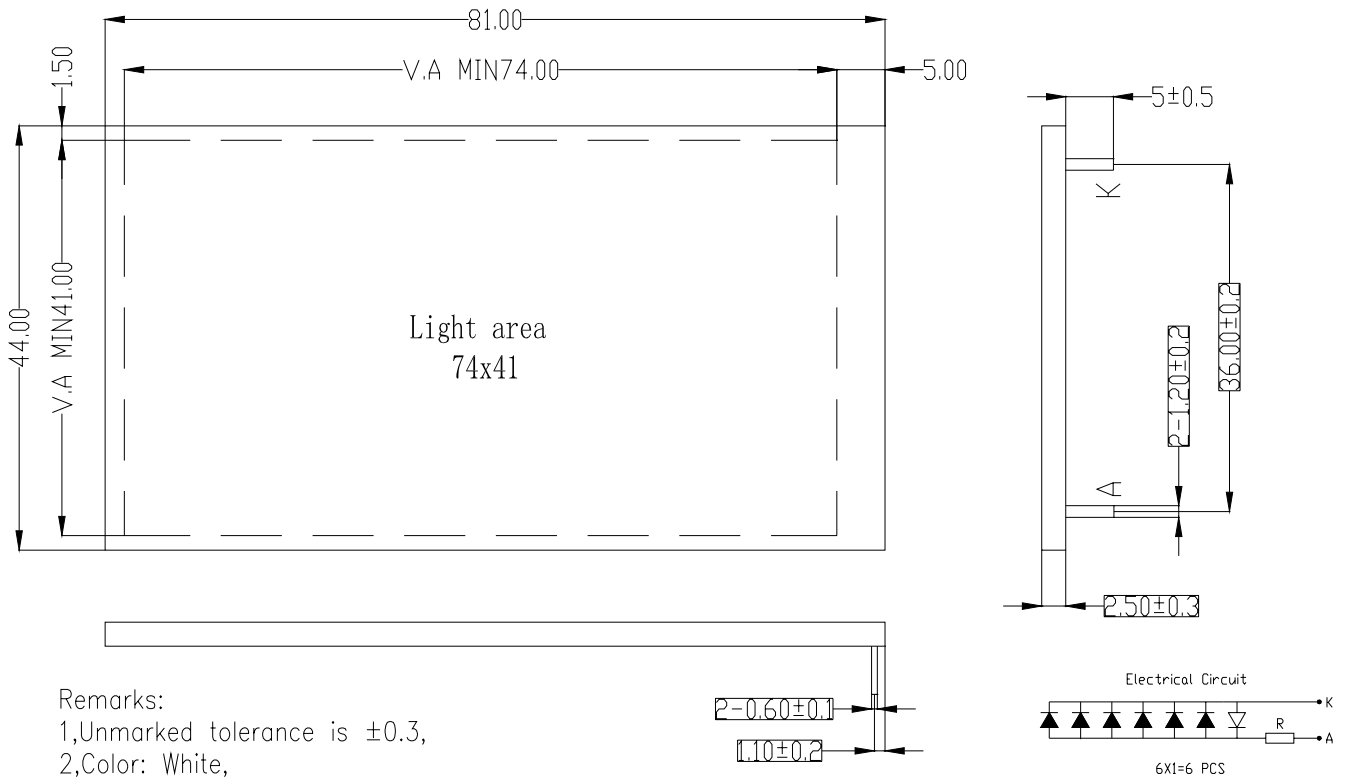


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8. BACKLIGHT ELECTRICAL/OPTICAL CHARACTERISTICS

Electronics/Optical Specifications:

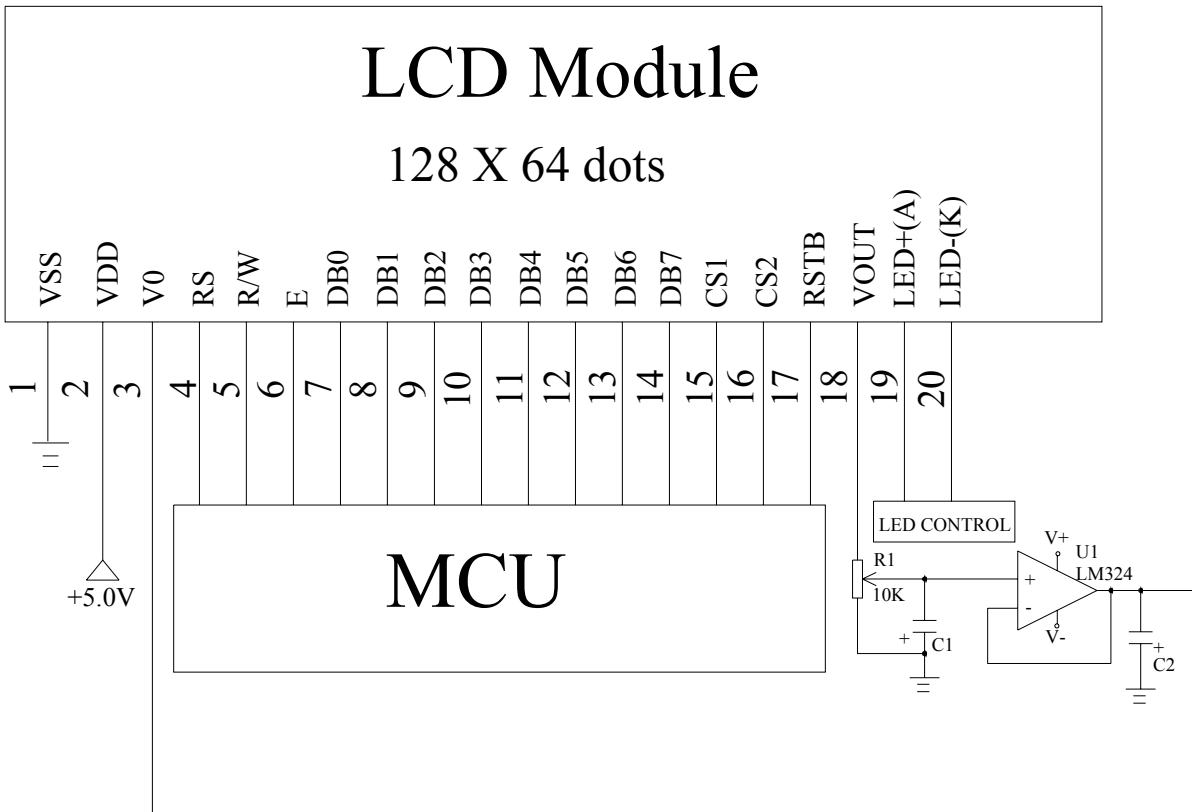
	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	V_f		4.0		V	
Forward Current	I_f		90	120	mA	$V_f = 4.0\text{ V}$
Power Dissipation	P_d		0.36		W	$V_f = 4.0\text{ V}$
Reverse Voltage	V_r			5.0	V	
Reverse Current	I_r			0.4	mA	
Luminous Intensity	L_v	150	250		cd/m ²	$V_f = 4.0\text{ V}$
Luminous Uniformity	ΔL_v	70			%	$V_f = 4.0\text{ V}$
Emission Wavelength	X	0.27		0.32		$I_f = 20\text{ mA}$ $T_a = 25^\circ$ Each chip
	Y	0.27		0.32		



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9. APPLICATION CIRCUIT



NOTE: 1. R1 is the contrast resistor.

2. VOUT=-9.5V

3. Adjust R1, it will be best contrast when V0 is -7.9V.

10. MAXIMUM ABSOLUTE POWER RATINGS (Ta=25°C)

Item	Symbol	Standard value	Unit
Supply voltage for logic	V _{DD}	-0.3~+7.0	V
Supply voltage	V _{EE}	VDD-16 (MIN.)	V
Driver supply voltage	V ₀ -V ₅	13 (MAX.)	V
Operating temperature	T _{opr}	-20~+70	°C
Storage temperature	T _{stg}	-25~+75	°C

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11. ELECTRICAL CHARACTERISTICS

11-1 DC Characteristics ($V_{DD}=5V, V_{SS}=0V, T_a=25^\circ C$)

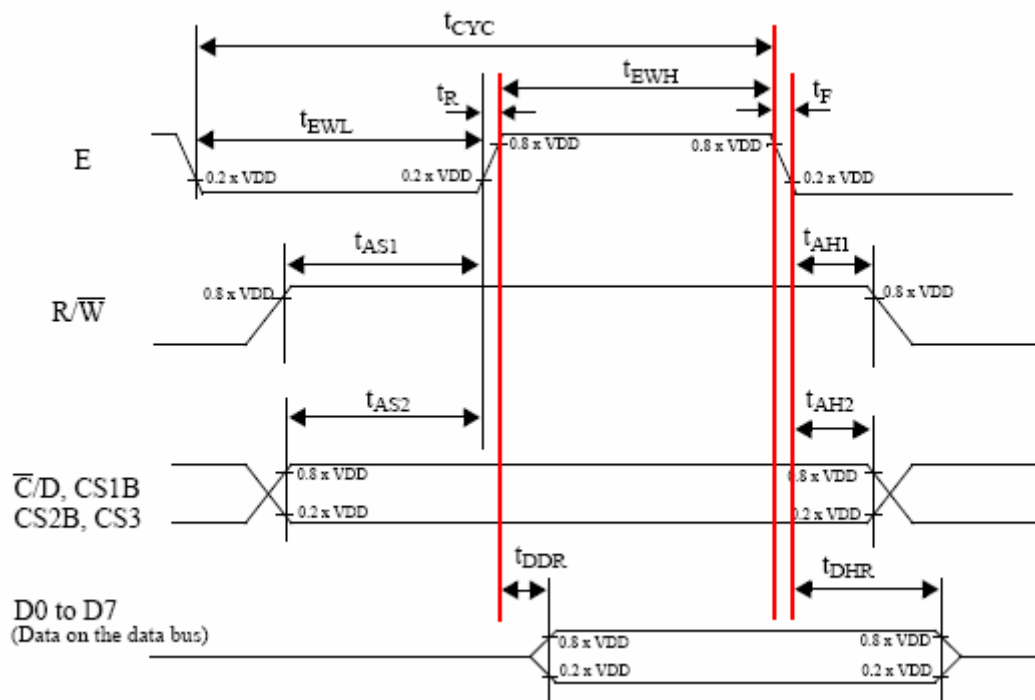
Item	Symbol	Standard Value			Test Condition	Unit
		MIN	TYP	MAX		
Supply current for logic	V_{DD}	4.7	5.0	5.3	-----	V
Supply current for logic	I_{DD}	----	TBD	----	-----	mA
Supply current for LCD	V_{LCD}	12.7	12.9	13.0	25°C	

11-2 AC Characteristics

11-2-1. AC timing for writing to the SBN0064G

($V_{DD} = 5 V ; V_{SS} = 0 V ; T_{amb} = 25^\circ C.$)

symbol	parameter	min.	max.	test conditions	unit
t_{CYC}	Enable (E) cycle time	1000			ns
t_{EWL}	Enable (E) LOW width	450			
t_{EWH}	Enable (E) HIGH width	450			
t_R	Enable (R) rise time		20		
t_F	Enable (F) fall time		20		
t_{AS1}	Write set-up time	140			
t_{AH1}	Write hold time	10			
t_{AS2}	C/D, CS1B, CS2B, CS3 set-up time	140			
t_{AH2}	C/D, CS1B, CS2B, CS3 hold time	10			
t_{DSW}	Data setup time (on the data bus)	200		The loading on the data bus is shown in Fig. 18.	
t_{DHW}	Data hold time (on the data bus)	10			



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11-2-2. AC timing for reading from the SBN0064G

(VDD = 5 V; VSS = 0 V; Tamb = 25°C.)

symbol	parameter	min.	max.	test conditions	unit
t_{CYC}	Enable (E) cycle time	1000			ns
t_{EWL}	Enable (E) LOW width	450			
t_{EWH}	Enable (E) HIGH width	450			
t_R	Enable (R) rise time		20		
t_F	Enable (F) fall time		20		
t_{AS1}	READ set-up time	140			
t_{AH1}	READ hold time	20			
t_{AS2}	C/D, CS1B, CS2B, CS3 set-up time	140			
t_{AH2}	C/D, CS1B, CS2B, CS3 hold time	10			
t_{DDR}	Data delay time (on the data bus)	320		The loading on the data bus is shown in Fig. 18.	
t_{DHR}	Data hold time (on the data bus)	20			

