

**Hungarydisplay**

**LCD**

**HDEM 160506**  
**LCD alfanumerikus**  
**STN Negative 16x2**

# Hungarydisplay

## 5. DC Electrical Characteristics

( TA = -30°C to 85°C, VDD = 2.7 V – 4.5 V )

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	-	2.7	-	4.5	V
V <sub>LCD</sub>	LCD Voltage	V0-Vss	2.7	-	7.0	V
I <sub>CC</sub>	Power Supply Current	VDD=3.0V (Use internal booster/follower circuit)	-	160	230	uA
V <sub>IH1</sub>	Input High Voltage (Except OSC1)	-	1.9	-	VDD	V
V <sub>IL1</sub>	Input Low Voltage (Except OSC1)	-	- 0.3	-	0.8	V
V <sub>IH2</sub>	Input High Voltage (OSC1)	-	0.7 VDD	-	VDD	V
V <sub>IL2</sub>	Input Low Voltage (OSC1)	-	-	-	0.2 VDD	V
V <sub>OH1</sub>	Output High Voltage (DB0 - DB7)	I <sub>OH</sub> = -1.0mA	0.75 VDD	-	-	V
V <sub>OL1</sub>	Output Low Voltage (DB0 - DB7)	I <sub>OL</sub> = 1.0mA	-	-	0.8	V
V <sub>OH2</sub>	Output High Voltage (Except DB0 - DB7)	I <sub>OH</sub> = -0.04mA	0.8 VDD	-	VDD	V
V <sub>OL2</sub>	Output Low Voltage (Except DB0 - DB7)	I <sub>OL</sub> = 0.04mA	-	-	0.2 VDD	V
R <sub>COM</sub>	Common Resistance	V <sub>LCD</sub> = 4V, I <sub>d</sub> = 0.05mA	-	2	20	KΩ
R <sub>SEG</sub>	Segment Resistance	V <sub>LCD</sub> = 4V, I <sub>d</sub> = 0.05mA	-	2	30	KΩ
I <sub>LEAK</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to VDD	-1	-	1	μA
I <sub>PUP</sub>	Pull Up MOS Current	VDD = 3V	20	30	40	μA
fOSC	Oscillation frequency	VDD = 3V, 1/17duty	350	540	1100	KHz

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( TA = -30°C to 85°C, VDD = 4.5 V - 5.5 V )

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	-	4.5	-	5.5	V
V <sub>LCD</sub>	LCD Voltage	V0-Vss	2.7	-	7.0	V
I <sub>CC</sub>	Power Supply Current	VDD=5.0V (Use internal booster/follower circuit)	-	240	340	uA
V <sub>IH1</sub>	Input High Voltage (Except OSC1)	-	2.7	-	VDD	V
V <sub>IL1</sub>	Input Low Voltage (Except OSC1)	-	-0.3	-	0.8	V
V <sub>IH2</sub>	Input High Voltage (OSC1)	-	0.7 VDD	-	VDD	V
V <sub>IL2</sub>	Input Low Voltage (OSC1)	-	-	-	1.0	V
V <sub>OH1</sub>	Output High Voltage (DB0 - DB7)	I <sub>OH</sub> = -1.0mA	3.8	-	VDD	V
V <sub>OL1</sub>	Output Low Voltage (DB0 - DB7)	I <sub>OL</sub> = 1.0mA	-	-	0.8	V
V <sub>OH2</sub>	Output High Voltage (Except DB0 - DB7)	I <sub>OH</sub> = -0.04mA	0.8 VDD	-	VDD	V
V <sub>OL2</sub>	Output Low Voltage (Except DB0 - DB7)	I <sub>OL</sub> = 0.04mA	-	-	0.2 VDD	V
R <sub>COM</sub>	Common Resistance	V <sub>LCD</sub> = 4V, I <sub>d</sub> = 0.05mA	-	2	20	KΩ
R <sub>SEG</sub>	Segment Resistance	V <sub>LCD</sub> = 4V, I <sub>d</sub> = 0.05mA	-	2	30	KΩ
I <sub>LEAK</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to VDD	-1	-	1	μA
I <sub>PUP</sub>	Pull Up MOS Current	VDD = 5V	65	95	125	μA
fOSC	Oscillation frequency	VDD = 5V, 1/17duty	350	540	1100	KHz

## 6. Optical Characteristics

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1/16 duty, 1/5 bias,  $V_{lcd}=4.5V$ ,  $T_a=25^\circ C$

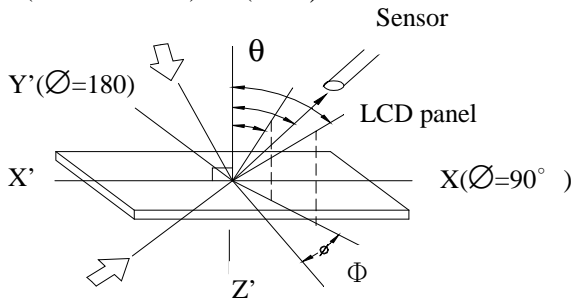
Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Driving Voltage	$V_{lcd}=V_{DD}-V_O$		4.2	4.5	4.8	V
	$V_{lcd}$	$-20^\circ C$	4.32	4.62	4.92	V
		$+25^\circ C$	4.2	4.5	4.8	V
		$+70^\circ C$	4.07	4.37	4.67	V
Viewing Angle	$\theta$	$C \geq 2.0, \phi = 0^\circ C$	$30^\circ$	-	-	Notes 1 & 2
Contrast	C	$\theta = 5^\circ, \phi = 0^\circ$	3.0	-	-	Note 3
Response Time(rise)	$t_{on}$	$\theta = 5^\circ, \phi = 0^\circ$	-	-	240ms	Note 4
Response Time(fall)	$t_{off}$	$\theta = 5^\circ, \phi = 0^\circ$	-	-	220ms	Note 4

Note 1: Definition of angles  $\theta$  and  $\phi$

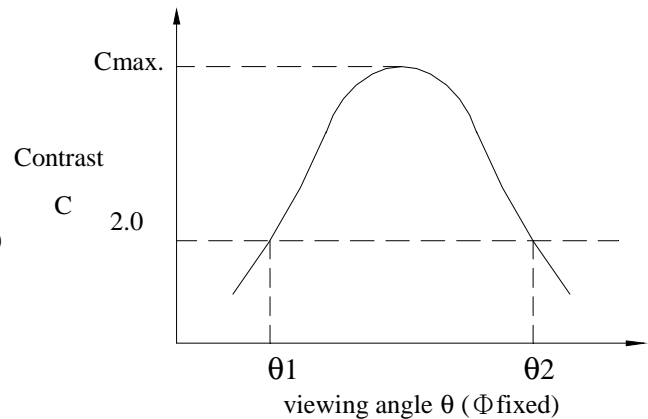
Note 2: Definition of viewing angles  $\theta_1$  and  $\theta_2$

$\phi$

Light (when reflected)  $z (\theta=0^\circ)$



Light (when transmitted)  $Y (\phi=0^\circ)$   
 $(\theta=90^\circ)$

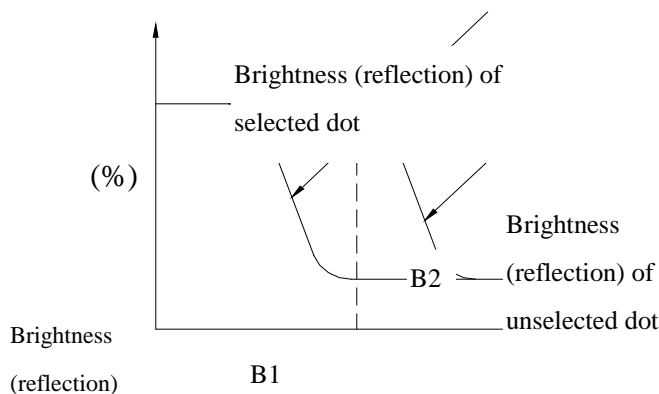


Note : Optimum viewing angle with the naked eye and viewing angle  $\theta$  at  $C_{max}$ . Above are not always the same

Note 3: Definition of contrast C

Note 4: Definition of response time

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$

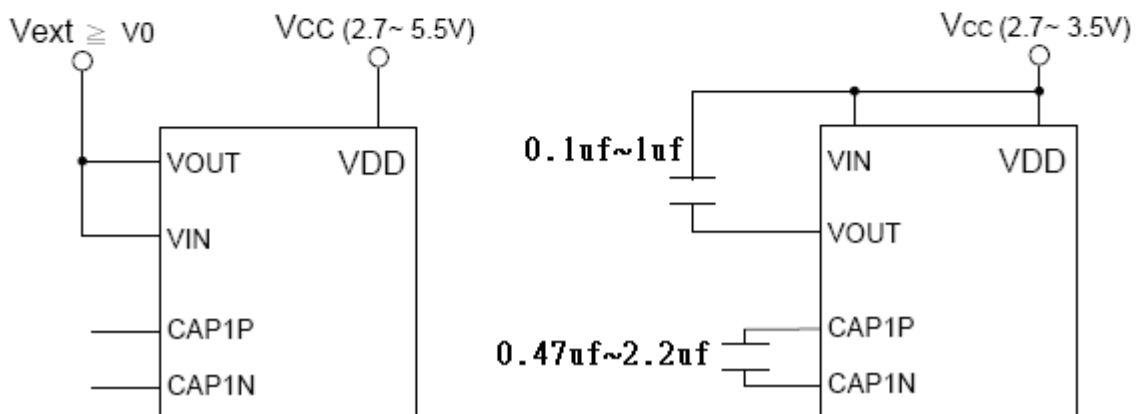
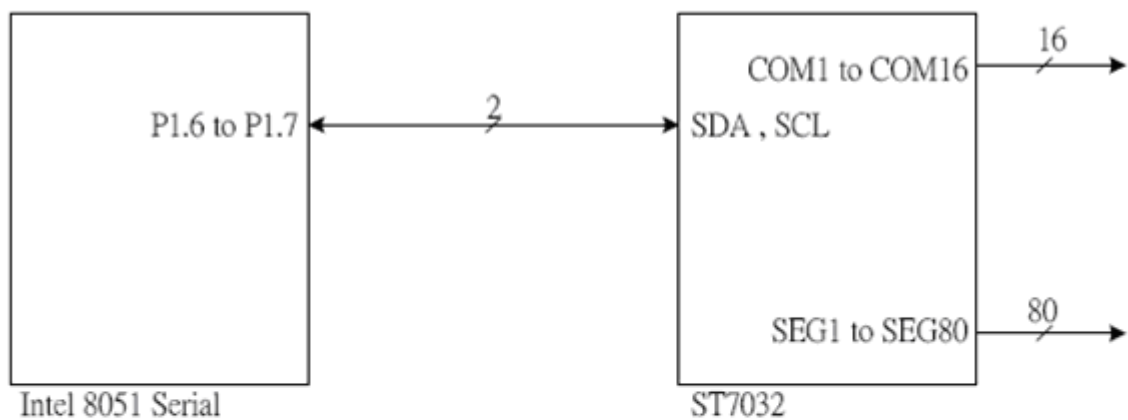


## 7. Interface Pin Description

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NO.	Symbol	Function
1	Vout	DC/DC voltage converter. Connect a capacity between this terminal and VDD when the built-in booster is used.
2	CAP1-	For voltage booster circuit(VDD-VSS) External capacitor about 0.1u~4.7uf
3	CAP1+	
4	VDD	Power Supply
5	VSS	Ground
6	SDA	Serial Data I/O
7	SCL	Serial Clock Input
8	RST	Reset Signal Input(Active Low)

### Intel 8051 interface( i<sup>2</sup>C )



## 8. RELIABILITY

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### 8.1 Reliability

Test item	Test condition	Evaluation and assessment
Operation at high temperature and humidity	40 °C±2 °C 90%RH for 500hours	No abnormalities in functions* and appearance**
Operation at high temperature	60 °C±2 °C for 500 hours	No abnormalities in functions* and appearance**
Heat shock	-20± ~ +60 °C Left for 1 hour at each temperature, transition time 5 min, repeated 10times	No abnormalities in functions* and appearance**
Low temperature	-20±2 °C for 500 hours	No abnormalities in functions* and appearance**
Vibration	Sweep for 1 min at 10 Hz, 55Hz, 10Hz, amplitude 1.5mm 2 hrs each in the X,Y and Z directions	No abnormalities in functions* and appearance**
Drop shock	Dropped onto a board from a height of 10cm	No abnormalities in functions* and appearance**

\* Dissipation current, contrast and display functions

\*\* Polarizing filter deterioration, other appearance defects

### 8.2 Liquid crystal panel service life

100,000 hours minimum at 25 °C±10 °C

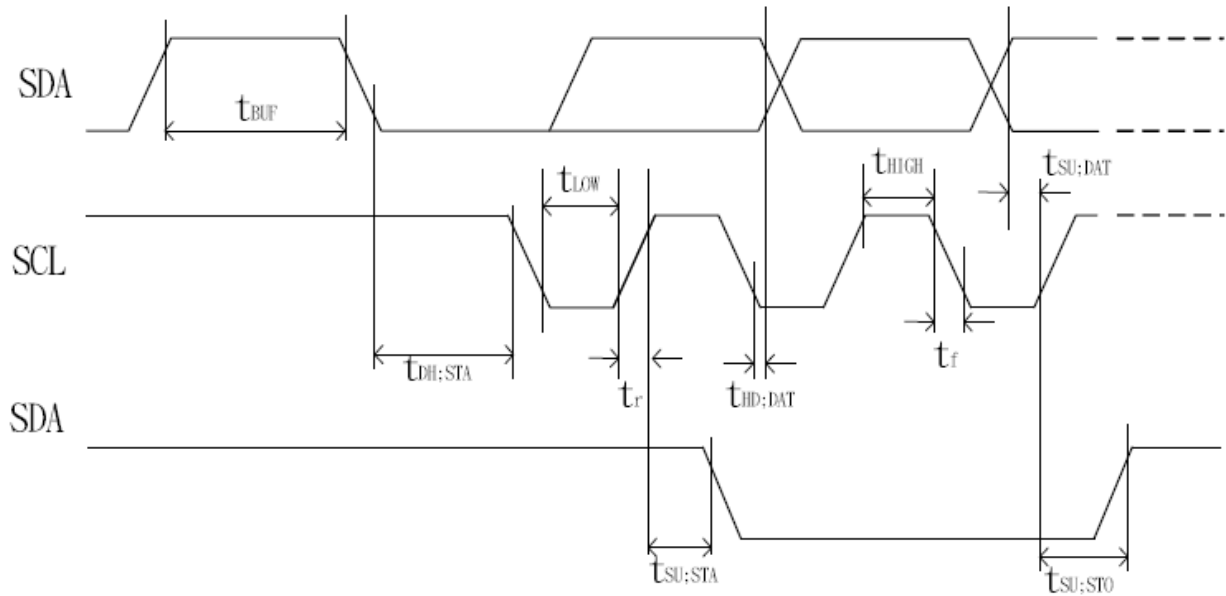
### 8.3 Definition of panel service life

- l Contrast becomes 30% of initial value
- l Current consumption becomes three times higher than initial value
- l Remarkable alignment deterioration occurs in LCD cell layer
- l Unusual operation occurs in display functions

## 9. Timing Characteristics

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- I2C interface



( Ta = -30°C to 85°C )

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	$f_{SCLK}$	—	DC	400	DC	400	KHz
SCL clock low period		$t_{LOW}$	—	1.3	—	1.3	—	us
SCL clock high period		$t_{HIGH}$	—	0.6	—	0.6	—	us
Data set-up time	SI	$t_{SU:DAT}$	—	<b>180</b>	—	100	—	ns
Data hold time		$t_{HD:DAT}$	—	0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	$t_r$	—	$20+0.1C_b$	300	$20+0.1C_b$	300	ns
SCL,SDA fall time		$t_f$	—	$20+0.1C_b$	300	$20+0.1C_b$	300	
Capacitive load represent by each bus line		$C_b$	—	—	400	—	400	pf
Setup time for a repeated START condition	SI	$t_{SU:STA}$	—	0.6	—	0.6	—	us
Start condition hold time		$t_{HD:STA}$	—	0.6	—	0.6	—	us
Setup time for STOP condition		$t_{SU:STO}$	—	0.6	—	0.6	—	us
Bus free time between a Stop and START condition	SCL	$t_{BUF}$	—	1.3	—	1.3	—	us

## 10. Display Command

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➤ instruction table at "Normal mode"

(When "EXT" option pin connect to VDD, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time			
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC=380KHz	OSC=540KHz	OSC=700KHz	
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	x	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	x	x	x	x	DL: interface data is 8/4 bits N: number of line is 2/1	26.3 us	18.5 us	14.3 us
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	AC0	Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	AC0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	D0	Write data into internal RAM (DDRAM/CGRAM)	26.3 us	18.5 us	14.3 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	D0	Read data from internal RAM (DDRAM/CGRAM)	26.3 us	18.5 us	14.3 us



# Hungarydisplay

## ➤ instruction table at "Extension mode"

(when "EXT" option pin connect to VSS, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC=380KHz	OSC=540kHz	OSC=700KHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	DH	*0	IS	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS: instruction table select	26.3 us	18.5 us	14.3 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us

Note \* : this bit is for test command , and must always set to "0"

### Instruction table 0(IS=0)

Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us

### Instruction table 1(IS=1)

Internal OSC frequency	0	0	0	0	0	1	BS	F2	F1	F0	BS=1:1/4 bias BS=0:1/5 bias F2~0: adjust internal OSC frequency for FR frequency.	26.3 us	18.5 us	14.3 us
Set ICON address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address in address counter.	26.3 us	18.5 us	14.3 us
Power/ICON control/Contrast set	0	0	0	1	0	1	Ion	Bon	C5	C4	Ion: ICON display on/off Bon: set booster circuit on/off C5,C4: Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us
Follower control	0	0	0	1	1	0	Fon	Rab2	Rab1	Rab0	Fon: set follower circuit on/off Rab2~0: select follower amplified ratio.	26.3 us	18.5 us	14.3 us
Contrast set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us